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Design and Testing of a Mixed Signal Matched Filter for IS-95 CDMA Code Acquisition

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ABSTRACT

Due to its advantages in multiple access, interference rejection, multipath mitigation, and access security, the direct-sequence spread spectrum (DS-SS) become very popular in mobile communication. For code acquisition of DS-SS signals, matched filters are the key components. This paper presents the design, implementation, and testing of a mixed signal matched filter. The proposed filter uses simple current mirrors to reduce the complexity of the crucial summation circuitry. The circuit is small in size and regular in structure; hence, one can cascade several to produce a filter of longer length. A 128-tap test chip has been implemented in a 2.5 mm^2 core by means of 0.8 μm SPDM digital CMOS technology. The DC and AC measurements confirm the feasibility of the design.

Key Words: matched filter, mixed signal design, VLSI, direct sequence spread spectrum, CDMA

I. Introduction

Code division multiple access (CDMA) is a modulation and multiple-access scheme based on spread-spectrum (SS) communication. The direct sequence spread-spectrum (DS-SS) modulates carriers by means of pseudorandom noise (PN) codes directly to spread the spectrum of the waveform (Pickholtz *et al.*, 1982; MaGill *et al.*, 1994). DS-SS provides an efficient means of multiple access, interference rejection, multipath mitigation, and access security. Hence, it has become popular in mobile communications. Prominent examples include the Global Positioning System (GPS), IS-95 personal communication system, and many satellite mobile phone systems, such as Globalstar by Loral/Qualcomm and Odyssey by TRW (MaGill *et al.*, 1994; Hinderling *et al.*, 1993).

For acquisition of DS-SS signals, matched filters are the key components. Matched filters compare the similarity between the receiving signal and the local PN code to indicate acquisition of the code. Since DS-SS signals are digital in nature, digital matched filters (DMF) provide a straightforward approach to obtaining correlation in code acquisition processors (Rappaport and Grieco, 1984; Hinderling *et al.*, 1993; Rose and Koether, 1990). They perform chip-by-chip coherent integration over all or part of the signal duration.

For rapid acquisition, parallel matched filters are often used (Pickholtz *et al.*, 1982; Rappaport and Grieco, 1984). A typical parallel digital matched filter (DMF) is shown in Fig. 1. A digital DMF is composed of two tapped delay lines, one for received data and another for local PN code, an array of multipliers for chip-by-chip correlation, and summation circuitry for integration. The tap length is chosen according to the system performance requirements (Pickholtz *et al.*, 1982; Polydoros and Weber, 1984). The longer the tap length is, the higher is the processing gain, the lower is the SNR, and the shorter is the acquisition time. However, increasing in tap length also increases the size and decreases the performance of the circuit. Here,

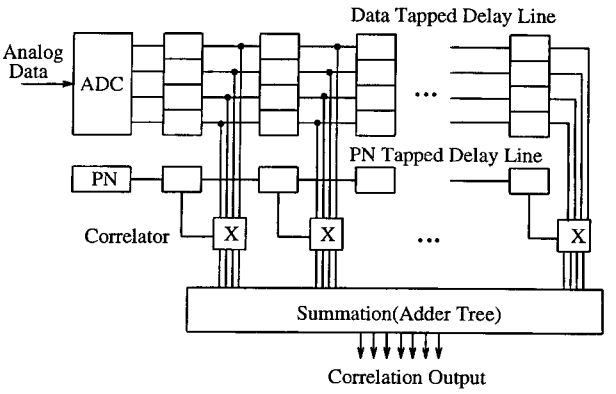

Fig. 1. Digital matched filter architecture.

area overhead and power consumption are two major considerations for mobile phones.

In this paper, we propose a mixed analog digital matched filter structure. The tapped delay lines and multipliers are implemented as digital circuits and the summation circuit as an array of simple digital to analog converters (DAC). The DACs convert the correlation results into analog currents to simplify the summation circuitry. In the following sections, we will describe the fundamental elements of DS-SS and matched filters in Section II, present the design and implementation of the circuit in Section III, give the measurement results of the chips in Section IV, and draw conclusions in Section V.

II. The Fundamentals of DS-SS and Matched Filters

1. Direct-Sequence Spread Spectrum System

In order to understand the functionality and performance requirements of the digital matched filter better, in this section, we will explain the basics of the DS-SS communication system. The spreading and despreading process differentiates DS-SS from conventional communication techniques. Figure 2 shows the spreading and despreading of the IS-95 DS-SS CDMA system (Hinderling *et al.*, 1993).

As Fig. 2 shows, each CDMA signal consists of a different PN code that modulates the carrier in order to spread the spectrum of the waveform. After the spreading process, narrow band user data is spread into a wideband SS signal. Different from time-division multiple access (TDMA) and frequency-division multiple access (FDMA), CDMA transmits multiple signals in the same frequency band at the same time. The desired signal is separated and retrieved through use of a correlator that accepts only the signal energy from the selected PN code. The signals from other users are treated as noise because their codes cannot be despreaded. The mathematical equations which represent the above concept are derived as follows.

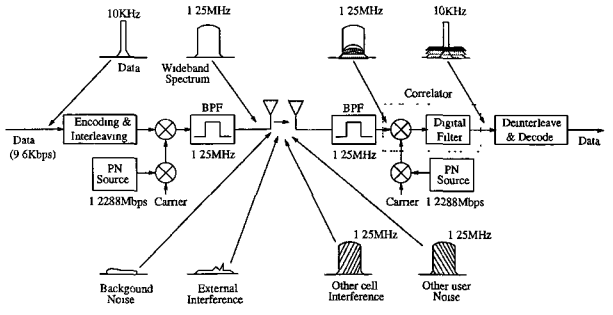

Fig. 2. A system overview of the direct sequence spread spectrum.

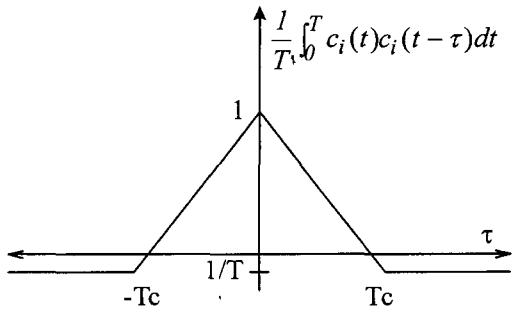

Fig. 3. Autocorrelation of a PN code.

Suppose that the data of the ith user is denoted as $d_i(t)$ and its PN code as $c_i(t)$. The transmitted signal of the ith user is

$$s_i(t)=d_i(t)\bullet c_i(t). \tag{1}$$

Since multiple users transmit in the same frequency band at the same time, the overall signal transmitted and received in a multiuser environment is

$$s(t)=\sum_{j=1}^{n} d_j(t)\bullet c_j(t). \tag{2}$$

At the receiving end, the received signal is despread by correlating it with the original spread signal $c_i(t)$:

$$r_i(t)=s(t)\bullet c_i(t)=\sum_{j=1}^{n} d_j(t)\bullet c_j(t)\bullet c_i(t). \tag{3}$$

Since the PN codes being used are equiprobable and equienergy orthogonal signals, they satisfy the following cross correlation property:

$$\int_0^T c_i(t)\bullet c_j(t)=\delta_{ij}=\begin{cases}1 & i=j\\ 0 & i\neq j\end{cases}. \tag{4}$$

Therefore, the result of this despreading process is

$$r_i(t)=d_i(t). \tag{5}$$

Such an ideal situation happens only when the local PN code is in perfect synchronization with the transmitting one. Otherwise, the despreaded signal $r_i(t)$ will be smaller. The amplitude is determined by the time offset τ. Here, τ is the timing difference between the local PN code and the transmitting PN code. The relationship is described as the autocorrelation of the PN code $c_i(t)$, shown in Fig. 3. The major consequence of the offset is a decrease of signal-to-noise ratio

(*SNR*).

If the local PN code is off by more than one chip time, the incoming signal will be no different from noise. In order to obtain synchronization, a DS-SS receiver often does it in two steps, code acquisition and code tracking. *Code acquisition* is employed to achieve coarse synchronization within one chip period, and *code tracking* is employed to fine tune the synchronization and maintain accurate timing thereafter. The key component in code acquisition is a matched filter, which performs chip-by-chip correlation of the local code and the received signal. In the discrete time domain, the correlation being performed is defined as

$$r_t(t) = \sum_{k=t-N}^{n} s(k) \cdot c_t(k). \qquad (6)$$

If the correlation result in Eq. (6) is greater than a predefined threshold value, then coarse synchronization is achieved. The synchronization is within a chip time, as Fig. 3 shows. The synchronization task is then handed over to a code tracking loop for further fine tuning. The crucial operation for hardware implementation of Eq. (6) is the summation function.

2. Matched Filter

Matched filters are divided into two classes, serial and parallel, according to the way in which correlation is performed. Serial matched filters perform correlation one chip at a time and use an integrator (accumulator) to obtain M-chip cross correlation over M chip time. Parallel matched filters perform M chip correlation simultaneously and use summation circuitry to obtain the M-chip cross correlation at every chip time. As one can see, serial matched filters have the advantages of low hardware complexity and flexible adjustment. By this we mean that the integration period can be changed easily. However, the acquisition time can be very long due to the serial property. On the other hand, parallel matched filters are much faster in terms of acquisition (Pickholtz *et al.*, 1982; Rappaport and Grieco, 1984; Rose and Koether, 1990). However, the hardware overhead can be excessive.

A parallel digital matched filter is required to calculate one sample of M-chip cross correlation in one chip time. The summation circuit is the critical module. The summation circuit can be implemented as an adder tree, systolic array, or bank-of-correlators (MaGill and Edwards, 1990; Kung, 1988). For a matched filter of very long tap length, hardware complexity and performance degradation become significant design challenges.

The design requirements for a matched filter of very long tap length are as follows. First, it must be regular in structure to minimize layout complexity. The ideal case is to implement it as an iterative array of identical cells such that one can cascade the same cells into a filter of longer length. Here, systolic arrays satisfy, but adder trees fall short in this category. Second, the cell structure must remain the same regardless of the tap length. Here, most digital designs must increase the bit number to avoid the overflow problem in the summation circuit if the tap length is increased. As a result, the cells must be altered accordingly. A simple guideline is to increase the bit number by one whenever the tap length is doubled. For example, for a 16-tap matched filter with 4-bit input data, the data width is 4 bits for the first stage, 5 bits for the second stage, 6 bits for stages 3 and 4, 7 bits for stages 5 to 8, and 8 bits for stages 9 to 16. Third, the circuit must be low in terms of power consumption in order for it to be used in a handset. Here, some low power design techniques must be used. In the next section, we will present our solution for meeting the above requirements.

III. Matched Filter Design and Implementation

1. Architecture Design

The proposed mixed analog digital matched filter is shown in Fig. 4. Here, we use digital to analog converters (DACs) to replace the summation circuit shown in Fig. 1. They convert digital correlation results into analog currents. As a result, we can use a single wire to sum up the correlation results. The important issue here is the design of the DACs. Their complexity determines their feasibility. Before we discuss the DACs, let us study the data format first. The inputs to the matched filter include local PN code

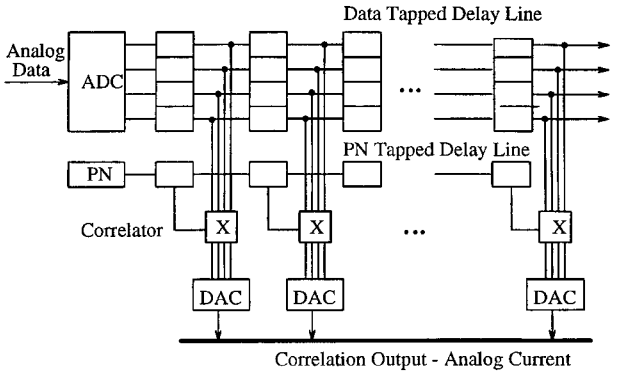

Fig. 4. Mixed signal matched filter architecture.

(PN) and the received data (S, D_2, D_1, D_0) in signed magnitude representation. Signed magnitude representation is used to simplify the correlation circuits. If the data is (1011), it is regarded -3 while (0011) is regarded +3. Note that an input bit length of 4 is selected according to the results obtained by Chen (1996). Here, 4-bit quantization is sufficient for code acquisition of IS-95 DS-SS signals using a 128-tap matched filter under an *SNR* of -17 dB.

2. Digital to Analog Converter

Since the application domain requires very long tap length, the DACs must be as simple as possible. Here, we propose use of simple current mirrors to convert digital signals into analog currents. Figure 5 shows the simple DAC implemented using current mirrors. The left three transistors produce the constant biasing voltages for the current mirrors on the right. They are shared by all the stages. The top and bottom three transistors are current mirrors, which produce positive and negative output currents in a power of 2. Transistors are sized in such a way that $I_{H1}=I_{L1}=I_{unit}$, $I_{H2}=I_{L2}=2I_{unit}$, and $I_{H4}=I_{L4}=4I_{unit}$. Here, I_{unit} is the unit current. I_{unit} is controlled by the biasing voltage, V_{bias}. The central six transistors controlled by H_i and L_i are switching transistors. When H_i is 0, it produces an output current of $i\times I_{unit}$. When L_i is 1, it produces an output current of $-i\times I_{unit}$. The final output current I_{out} is

$$I_{out}=I_{unit}\times(4\times\overline{H_4}-4\times L_4+2\times\overline{H_2}-2\times L_2+\overline{H_1}-L_1). \quad (7)$$

3. Correlator Design

In order to switch the currents, the correlator must produce six signals (H_1, H_2, H_4, L_1, L_2, L_4) with the following function:

$$H_i=\overline{(PN\oplus S)D_i} \quad (8)$$

$$L_i=(\overline{PN\oplus S})D_i\ . \quad (9)$$

If PN and the data are of the same sign, PN is 1(0) and S is 0(1), and the correlation result is positive. Now, we must turn off all the N switches and turn on the P switches according to D_is. Since a P switch is turned on by a 0, H_i is equal to $\overline{D_i}$. Similarly, when PN and the data have different signs, PN is 1(0) and S is 1(0). In this case, the H_i s must all be 1s to turn off P switches, and L_i is equal to D_i. The truth table of the correlator is shown in Table 1.

The extra control line, *Ctrl*, in Fig. 6 controls the conduction angles of the current mirrors. It serves two special purposes. First, it can be used as an automatic gain control (AGC) ADC, which is desirable in wireless communication. Second, it can be used to control the average current and power consumption. The proposed design uses only 12 transistors per stage, which is negligible as compared to the 10-bit adder used in the all-digital design. Now that we have presented the design, in the next section, we will present the chip implementation and post layout simulation results.

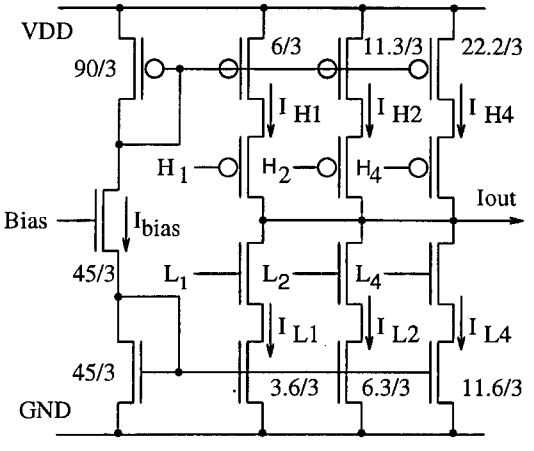

Fig. 5. Current mirrors as DAC.

Table 1. Correlation Circuit Truth Table

PN	S	H_i	L_i
0	0	1	D_i
0	1	$\overline{D_i}$	0
1	0	$\overline{D_i}$	0
1	1	1	D_i

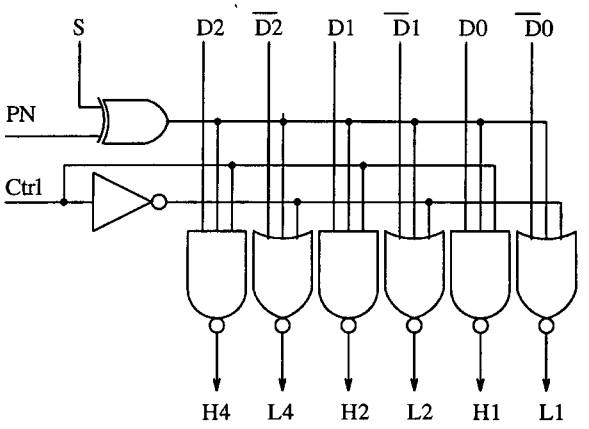

Fig. 6. Correlator circuit diagram.

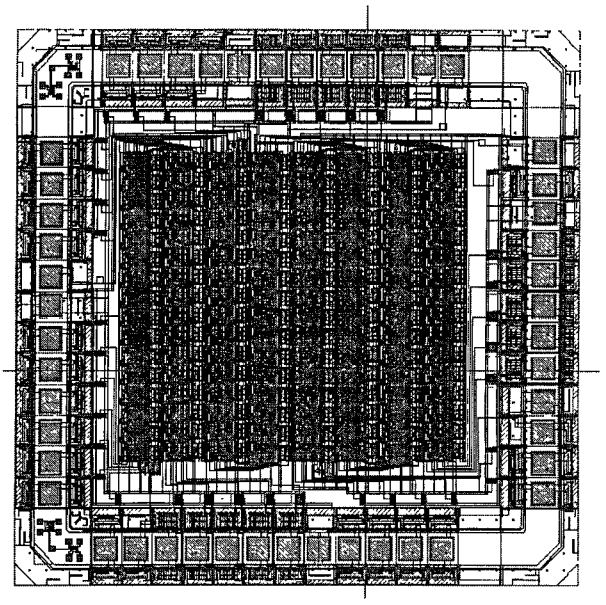

Fig. 7. Chip layout.

Table 2. Chip Summary

Chip Area	2.6×2.7 mm^2
Core Area	1.5×1.65 mm^2
Transistor Count	17191
Pin Count	48
Total Tap Length	128
Data Bit Width	4 bits
PN Code Bit Width	1 bit
Power Supply	2V
Measured Power Consumption	5.6 mW (chip)
Specification Chip Rate	1.2288 Mcps
Maximal Chip Rate Tested	10 Mcps

4. Chip Layout

The chip is implemented by means of TSMC 0.8 μm SPDM digital CMOS technology using the Cadence OPUS system. Figure 7 shows the layout of the whole chip. It consists of eight banks of 16-stage matched filters. These matched filters are configured as three matched filters, one 64-tap filter and two 32-tap filters. The core with a total of 128 taps occupies an area of 1.5 mm by 1.65 mm. The chip summary is given in Table 2.

5. Post Layout Simulation

After obtaining the layout, we extract the circuit-level SPICE parameter using the Dracula parameter extraction program to run a post layout simulation. From the post layout simulation, we are able to determine the performance of the circuit and verify the design and layout more accurately.

As mentioned earlier, V_{bias} is chosen to obtain a compromise between the linearity of current mirroring and power consumption. After obtaining the layout, we extract the circuit parameters and parasitics and use HSPICE to do the post layout simulation. Figure 8 shows the HSPICE simulation of I_{H1} and I_{L1} as a function of V_{bias}. As one can see, we have an acceptable linear region for V_{bias} between 1.6 V and 1.8 V. Therefore, V_{bias} is selected as 1.7 V. Under a V_{bias} of 1.7 V, I_{H1} and I_{L1} are both 600 nA.

For this circuit, the output voltage varies depending on the output current because the sink is unlikely to have a load resistance of 0 Ω. It is clear that the output offset voltage will affect the current mirroring effects. Figure 9 shows the HSPICE simulation of I_{Hi} s and I_{Li} s as a function of V_{offset} when V_{bias} is 1.7 V. For V_{offset} changes from 0.2 V to 1.7 V, the output currents remain constant. Our measurement of the

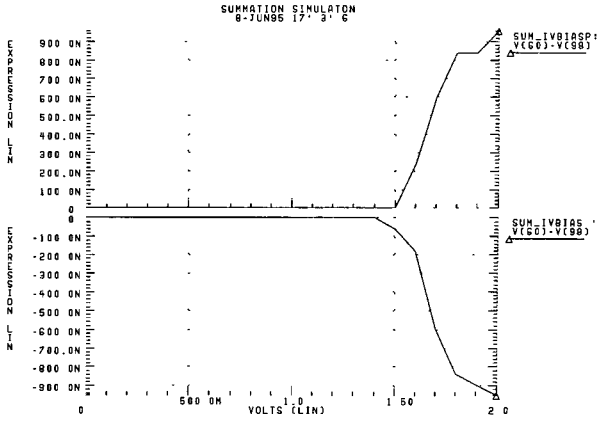

Fig. 8. I_{H1} and I_{L1} v.s. V_{bias}.

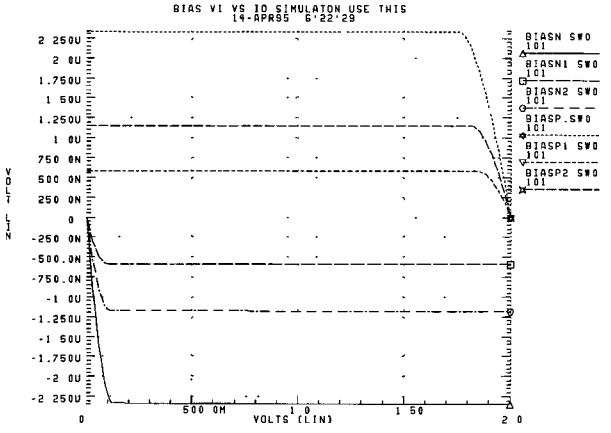

Fig. 9. Output currents v.s. V_{offset}.

Table 3. Measured Output Current in μA with Individual V_{bias} Adjustment

Case #	V_{bias}	I_{H1}	I_{H2}	I_{H4}	I_{L1}	I_{L2}	I_{L4}
1	1.72V	0.576	1.224	2.612	0.700	1.464	3.024
2	1.74V	0.576	1.212	2.600	0.723	1.564	3.136
3	1.75V	0.564	1.236	2.636	0.636	1.332	2.764
4	1.76V	0.564	1.224	2.600	0.712	1.512	3.088
5	1.78V	0.576	1.224	2.600	0.724	1.576	3.224
6	1.78V	0.576	1.236	2.576	0.636	1.400	2.888
7	1.78V	0.576	1.224	2.600	0.700	1.536	3.124
8	1.79V	0.576	1.212	2.588	0.724	1.548	3.152

fabricated chips does show this property. This is quite a wide linear region for a 2 V power supply.

IV. Measurement and Test Results

1. DC Measurement

After fabrication was completed, the measurement results of eight out of ten sample chips were as follows. For a V_{bias} of 1.7 V, I_{H1} ranged from 0.288 μA to 0.48 μA and I_{L1} from 0.348 μA to 0.56 μA under a V_{bias} of 1.7 V. As expected, the output current remained unchanged for a V_{offset} of 0.2 V to 1.7 V. Note that the chip was implemented using a digital process; hence, such variation is acceptable. If we adjusted V_{bias} individually, the output currents were much more stable. Table 3 shows the DC measurements of the eight chips with V_{bias} adjusted individually to have the same I_{H1}. As one can see, very consistent results were obtained after the individual adjustment. Note that, since the current was too small to measure, the results are the average of 32 stages.

The measured results suggest that further fine tuning is required. First, there is a nonlinearity problem; I_{H2} and I_{H4} are not exactly two and four times I_{H1}. Second, there is a mismatch problem; I_{H1} is not equal to I_{L1}. The first problem can be corrected through transistor sizing and the second by controlling the biasing voltages of the P and N mirrors individually. Otherwise, one can build an OP inside to control the current automatically. The above measurements were static measurements. In the following, we will present the dynamic measurements.

2. Dynamic Linearity Measurement

As shown in Fig. 10, we activated and disabled one tap at a time to create a triangular waveform to show the linearity of the current mirrors. The PN code was given a constant of all 1's. The data tap delay line was reset to 0 initially. Then, 32 chips of 1s were shifted in, followed by 32 chips of 1s, to create a triangular waveform. Figure 10 shows the results when ±1s were shifted. As one can see, the upper and lower halves are not symmetric, as discussed earlier, while the linearity are preserved quite well in separate regions.

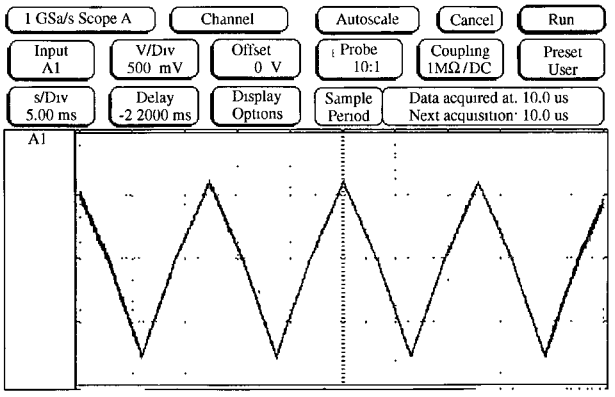

Fig. 10. Test result-linearity test (±1).

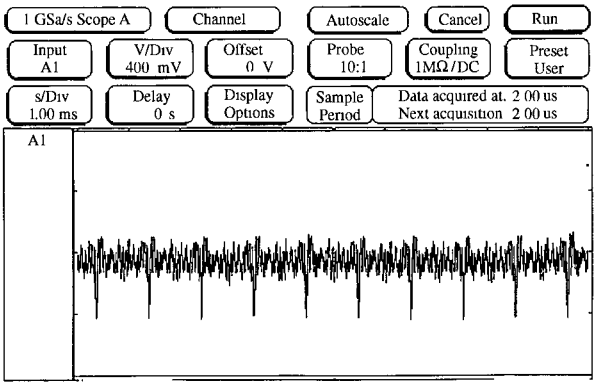

Fig. 11. Test result-32-tap matched filter.

3. Dynamic Random Data Measurement

We tested the filters using random data. We kept a PN code in the PN tap delay line. Then, we shifted a series of random data which contained the local PN code through the data tapped delay line. Figure 11 shows the output signal of a 32-tap matched filter. It is very close to the simulation results obtained using SPW. As stated earlier, one can cascade several matched filter into one of longer length. Figure 12 shows a diagram in which four 32-tap matched filters are cascaded to make one with 128 taps. We simply connect their data and PN tapped delay lines in serial and tie their current output lines together. Figure 13 shows the measurement results obtained by a 128-tap filter.

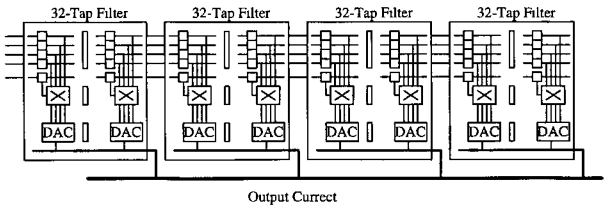

Fig. 12. Architecture of 128-tap MF-cascade of four 32-tap MF.

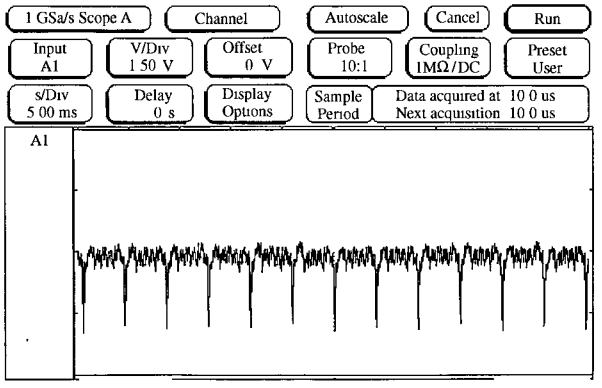

Fig. 13. Test result-128-tap matched filter (4x32-tap).

As expected, the signal to noise ration (*SNR*) increased when the tap length increased. Note that their vertical axes are in different scales. It is 400 mV per division for the 32-tap case and 1.5 V for the 128-tap case. With this example, we have shown how flexible our architecture is and how easy it can be reconfigured and expanded.

4. Multi-User Measurement

Furthermore, we tested the matched filter with multiple users. Figure 14 shows the test results for 4 equiprobable and equienergy users. This situation matches the situation of IS-95, where the pilot channel occupies one fourth of the transmitting power. As one can see, we still obtain enough *SNR* for code acquisition in this case.

V. Conclusions

In this paper, we have proposed a mixed signal matched filter for code acquisition in direct sequence spread spectrum systems. We use simple analog current mirrors to replace digital summation circuitry. As a result, the circuit complexity is reduced significantly. To show the feasibility of the design, we have implemented a 128-tap matched filter in 2.48 mm^2 using 0.8

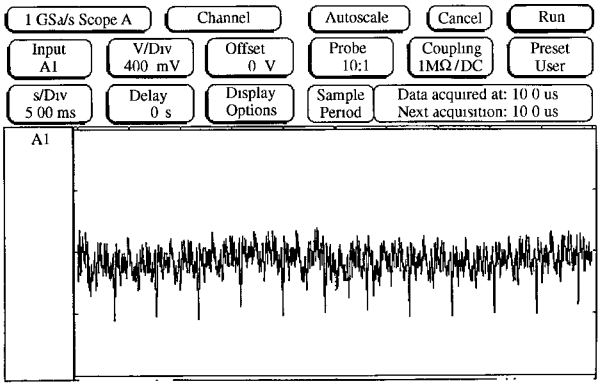

Fig. 14. Test result-128-tap matched filter (4 users).

μm SPDM digital CMOS technology. The chip has been tested thoroughly. All the measurements, DC, dynamic linearity, random data, and multi-user data, validate the design. The design is regular, flexible, small in size, and low in power consumption. Multiple matched filters can be cascaded to make a filter longer in length. These features make it especially suitable for implementing matched filters of very long tap length.

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適用於IS-95碼攫取之混合信號匹配濾波器

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摘　要

直接序列展頻技術已成爲行動通訊的主要方法。主要的原因，在於它能提供較佳的多工、干擾的豁免、以及通信的保密。在直接序列的碼獲取電路中，匹配濾波器爲一主要的元件。在此一論文中，我們將發表一個混合信號匹配濾波器的設計、製作、及測試。我們使用簡單的類比電流鏡電路，取代複雜的數位總合電路。此一電路具有規則、面積小、及彈性使用等的優點。因且我們可以將數個濾波器，串接成一個長度較長的濾波器。我們使用臺灣積體電路零點八微米的製程，製作了一個128級的匹配濾波器。該積體電路的直流與交流的測試，驗證了我們所提架構的可行性。