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# Two-dimensional Mixed-level Device and Circuit Simulation Using HSPICE

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## ABSTRACT

This paper presents an equivalent circuit approach to 2D numerical mixed-level device and circuit simulation using HSPICE. In this paper, Poisson's and continuity equations are formulated into a subcircuit format suitable for general circuit simulators such as HSPICE. In other words, the device is converted to an equivalent circuit model, which changes the device simulation problem into a circuit analysis problem and allows simultaneous solution of an electrical network containing both nonlinear circuit elements and numerical models of devices. Different from conventional approaches, our approach is conceptually simple, and the extension of this model to three-dimensional device simulation is straightforward. The utility of this approach in mixed-level simulation is demonstrated through transient analysis of diode switching circuit, SOS (semiconductor-oxide-semiconductor) test circuit and submicron MOSFET simulation using HSPICE.

**Key Words:** HSPICE, device simulation, SOS, MOSFET

## I. Introduction

Mixed-level device and circuit simulation is an increasingly important issue for efficient design and accurate simulation of integrated circuits. Because such mixed-level simulation provides a direct link between technology parameters and circuit performance, it is useful in predicting the effects that variations in technology and device designs have on circuit performance. Conventional device-level simulation, like PISCES, can typically model a single device in detail with fixed or predetermined boundary conditions. However, it cannot be used to evaluate the characteristics of the device under realistic dynamic boundary conditions imposed by a circuit.

In this paper, an equivalent circuit approach to two-dimensional numerical device/circuit mixed-level simulation using HSPICE is presented. Equivalent circuit approaches for semiconductor device simulation have been investigated by Chan and Sah (1979) and Sah (1987). Sah linearized the Shockley equations and synthesized the resulting difference equations into equivalent distributed circuits. Recently, some researchers have tried to develop new models and methods for mixed-level simulation (Leblebici *et al.*, 1992;

Unlu *et al.*, 1995; Wong and Chan, 1994). Basically, they also proposed ways to formulate the semiconductor equations into a format which fits existing simulators. However, in these classical transmission-line and node-by-node representations of the one-dimensional semiconductor equations, the equivalent circuit is usually characterized by a complicated structure and tedious derivation. On the contrary, our model is directly derived from the set of differential equations without complicated network topology or tedious derivation. The equivalent circuit model of the device can be directly linked with external circuit elements, which lends this approach to mixed-level simulation. Hence, it is easy to implement in many existing circuit simulation environments such as HSPICE. The algorithm of this method is shown by the flow chart in Fig. 1. We use the 'element-by-element' approach rather than 'node-by-node', and the new variables we use, defined as  $\psi$ ,  $\phi_n$ , and  $\phi_p$ , denote the electrostatic potential, the electron and hole quasi-Fermi potentials, respectively.

The rest of this paper is organized as follows. Section II gives the theory and the development of our new circuit model for 2D mixed-level simulation. In Section III, a diode switching circuit, SOS (semicon-

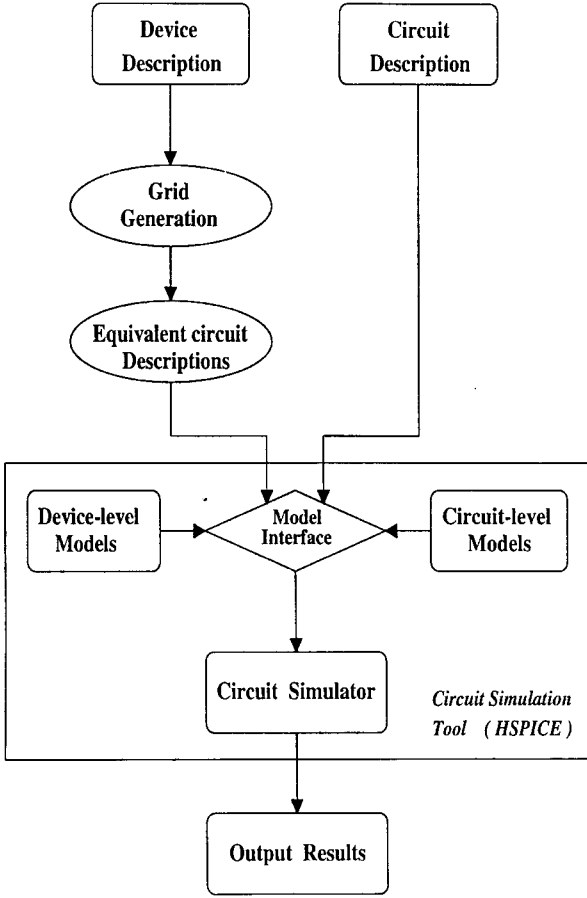


Fig. 1. The algorithm of the equivalent circuit approach to numerical mixed-level simulation.

ductor-oxide-semiconductor) test circuit and submicron MOSFET device are used as examples to demonstrate implementation of this modeling technique in HSPICE. Boundary conditions and current calculation are discussed in Section IV. Finally, conclusions are drawn in Section V.

## II. Model Development

In this section, the subcircuit model for two-dimensional mixed-level simulation will be developed. Usually, semiconductor behavior is governed by Poisson's and continuity equations. Most of the existing device simulators are based on the drift-diffusion (DD) description of carrier transport and employ specialized techniques to obtain one-, two-, or three-dimensional solutions in the time domain.

For two-dimensional device simulation, the simulation region can be partitioned into many meshes and nodes. One of the meshes is shown in Fig. 2. Carrier transport in semiconductors is described by three coupled partial differential equations,

namely, the Poisson equation, the electron-current continuity equation and the hole-current continuity equation:

$$\nabla^2 \psi = -\frac{q}{\epsilon} (p - n + N_D^+ - N_A^-) \quad (1)$$

$$-q \frac{\partial n}{\partial t} + \nabla \cdot \bar{J}_n = qR \quad (2)$$

$$q \frac{\partial p}{\partial t} + \nabla \cdot \bar{J}_p = -qR. \quad (3)$$

The auxiliary equations are:

$$\bar{J}_n = -q\mu_n n \nabla \psi + qD_n \nabla n \quad (4)$$

$$\bar{J}_p = -q\mu_p p \nabla \psi - qD_p \nabla p, \quad (5)$$

where  $J_n$  and  $J_p$  include the drift and diffusion components and are functions of  $(\psi, n, p)$ . Furthermore, we neglect the effects of bandgap narrowing, that is,  $\bar{E}_n = \bar{E}_p = \bar{E} = -\nabla \psi$  (electric field) and assume Boltzmann carrier statistics. For the range of operation of most semiconductor devices, the carrier concentrations can be simplified as

$$n \approx N_C \exp(\eta_n) = n_{ie} \exp[(\psi - \phi_n)/\phi T] \quad (6)$$

$$p \approx N_V \exp(\eta_p) = n_{ie} \exp[(\phi_p - \psi)/\phi T], \quad (7)$$

where  $\psi$ ,  $\phi_n$ , and  $\phi_p$  are the electrostatic potential, the electron quasi-Fermi potential, and the hole quasi-Fermi potential, respectively.  $(N_D^+ - N_A^-)$  is the ionized impurity concentration. Each notation in the above equations has its usual meaning. For subcircuit modeling, the unknown variables should be compatible with node voltage in circuit simulation. Hence, we choose  $\psi$ ,  $\phi_n$ ,

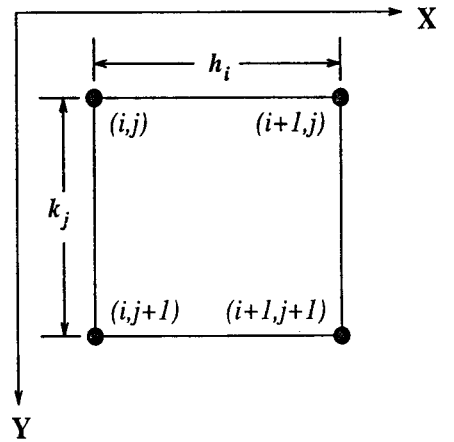


Fig. 2. A rectangular mesh in two-dimensional simulation.

and  $\phi_p$  instead of the usual variables,  $\psi$ ,  $n$ , and  $p$ . However, the two sets of variables can be calculated from each other.

The *Green theorem* can be used to discretize the Poisson equation. In an element as shown in Fig. 2, Eq. (1) can be rewritten as follows.

At node  $(i,j)$ :

$$\lambda^2 \frac{\psi_{ij} - \psi_{i+1,j}}{h_i} \cdot \frac{k_j}{2} + \lambda^2 \frac{\psi_{ij} - \psi_{i,j+1}}{k_j} \cdot \frac{h_i}{2} + (n - p - C)_{ij} \cdot \frac{h_i}{2} \cdot \frac{k_j}{2} = 0, \quad (8)$$

where  $\lambda^2 = \epsilon/q$  and  $C = N_D^+ - N_A^-$ . Equation (8) can be further simplified as

$$I_{R\psi_1} + I_{R\psi_2} + I_{\psi_3} = 0, \quad (9)$$

where

$$I_{R\psi_1} = \lambda^2 \frac{\psi_{ij} - \psi_{i+1,j}}{h_i} \cdot \frac{k_j}{2} = \frac{\psi_{ij} - \psi_{i+1,j}}{R_{\psi_1}} \quad (10)$$

$$I_{R\psi_2} = \lambda^2 \frac{\psi_{ij} - \psi_{i,j+1}}{k_j} \cdot \frac{h_i}{2} = \frac{\psi_{ij} - \psi_{i,j+1}}{R_{\psi_2}} \quad (11)$$

$$I_{\psi_3} = (n - p - C)_{ij} \cdot \frac{h_i}{2} \cdot \frac{k_j}{2} \quad (12)$$

Note that  $R_{\psi_1}$  and  $R_{\psi_2}$  describe the equivalent resistors in the circuit model, and that  $I_{\psi_3}$  describes a non-linear voltage-dependent current source. The above equivalent currents are supposed to be based on unit width, and the equivalent circuit is shown in Fig. 3. Likewise,  $I_{\psi_2}$ ,  $I_{\psi_3}$ ,  $I_{\psi_4}$ ,  $R_{\psi_3}$ , and  $R_{\psi_4}$  can be obtained in the same way. The subcircuit in this element can be implemented into a circuit simulator by means of the eight model components, one element at a time.

Next, the equivalent circuit for the electron continuity equation can be written as follows.

At node  $i$ :

$$I_{n1} + I_{n2} + I_{n3} + I_{n4} = 0, \quad (13)$$

where

$$I_{n1} = -qD_{n,i+1/2,j} \cdot \frac{B(x_{b,i+1/2,j}) \cdot n_{ij} - B(-x_{b,i+1/2,j}) \cdot n_{i+1,j}}{h_i} \cdot \frac{k_j}{2} \quad (14)$$

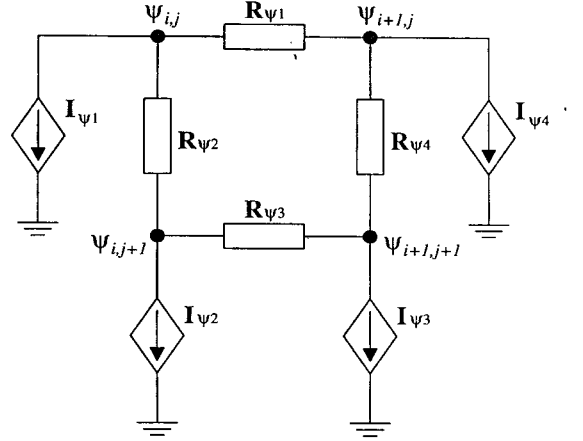


Fig. 3. An equivalent circuit corresponding to the Poisson's equation.

$$I_{n2} = -qD_{n,i,j+1/2}$$

$$\cdot \frac{B(x_{b,i,j+1/2}) \cdot n_{ij} - B(-x_{b,i,j+1/2}) \cdot n_{i,j+1}}{k_j} \cdot \frac{h_i}{2} \quad (15)$$

$$I_{n3} = -qR_i \cdot \frac{h_i}{2} \cdot \frac{k_j}{2} \quad (16)$$

$$I_{n4} = -q \frac{\partial n_{ij}}{\partial t} \cdot \frac{h_i}{2} \cdot \frac{k_j}{2} = C(\psi_{ij} - \phi_{n,ij}) \cdot \frac{\partial(\phi_{n,ij} - \psi_{ij})}{\partial t} \quad (17)$$

Note that  $x_{b,i+1/2,j}$  in  $I_{n1}$  is given as follows:

$$x_{b,i+1/2,j} = (\psi_{ij} - \psi_{i+1,j}) / \phi T. \quad (18)$$

$B(x_b)$  is the Bernoulli function, which is defined as

$$B(x_b) = \frac{x_b}{e^{x_b} - 1}. \quad (19)$$

The recombination rate  $R$  is described by the well-known Shockley-Read-Hall model as

$$R = \frac{pn - n_{ie}^2}{\tau_p(n + n_{ie}) + \tau_n(p + n_{ie})}. \quad (20)$$

In Eq. (20), we assume that the trap center is located at the center of the forbidden gap.  $I_{n3}$  is a recombination current while  $I_{n4}$  is a nonlinear voltage-dependent current which can be implemented as a nonlinear capacitor.  $R_{ij}$  and  $n_{ij}$  are the recombination rate and the electron concentration at node  $(i,j)$ , respectively; they may include the three variables  $\psi$ ,  $\phi_n$ , and  $\phi_p$ . The equivalent circuit for the electron continuity equation is shown in

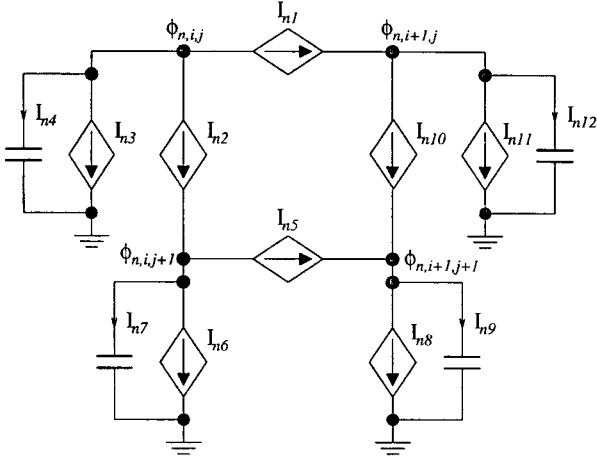


Fig. 4. An equivalent circuit corresponding to the electron continuity equation.

Fig. 4. Similarly, the equivalent circuit for the hole continuity equation can be written in the same way.

Semiconductor equations  $f_{V_i}$  can be solved by applying the Newton-Raphson iteration technique to the circuit model as

$$\frac{\partial f_{V_i}}{\partial V_i} \delta V_i = -f_{V_i} \quad (21)$$

or

$$A \delta V_i = b, \quad (22)$$

where  $V_i$  represents  $\psi$ ,  $\phi_n$ , or  $\phi_p$ .

### III. Boundary Condition and Current Calculation

In the following simulation examples, the boundary conditions are established based on only ohmic contact at the device terminals; i.e., the surface potential and electron and hole concentrations ( $\psi_s$ ,  $n_s$ ,  $p_s$ ) are fixed (Shur, 1990):

$$\phi_n = \phi_p = V_{\text{applied}} \quad (23)$$

$$n_s = \frac{1}{2}[(N_D^+ - N_A^-) + \sqrt{(N_D^+ - N_A^-)^2 + 4n_{ie}^2}] \quad (24)$$

$$p_s = \frac{n_{ie}^2}{n_s} \quad (25)$$

$$\psi_s = \phi_n + \frac{kT}{q} \ln \left( \frac{n_s}{n_{ie}} \right) = \phi_p - \frac{kT}{q} \ln \left( \frac{p_s}{n_{ie}} \right). \quad (26)$$

The electrostatic potential at the boundary is deter-

mined by the externally applied bias voltage, which, in turn, depends on the external load circuit. The modeling of the electrostatic potential boundary conditions is achieved by using a voltage-control voltage source. On the other hand, it is assumed that the equilibrium conditions are satisfied at the boundary.

The current density flow through the device consists of the displacement current density and the conduction current density. The total conduction current density across the device is found as the sum of the electron and hole current density,  $\bar{J}_n$  and  $\bar{J}_p$ . That is,

$$\bar{J}_c = \bar{J}_n(x_j) + \bar{J}_p(x_j). \quad (27)$$

The displacement current density for a given grid node can be computed directly by taking the time derivative of the local electric field:

$$\bar{J}_d = \epsilon \cdot \frac{d\bar{E}}{dt} = \epsilon \cdot \frac{d}{dt} \left( -\frac{d\psi}{dx} \right), \quad (28)$$

where  $\epsilon$  is the dielectric permittivity, and the electrical field,  $\bar{E}$ , is obtained by means of the difference between the electrostatic potentials in the neighboring nodes. In our circuit model, the current flow through the element  $i$  already includes the displacement current and the conduction current. This is because if we combine Eqs. (2) and (3) (which is the total current density), the result is the following relationship:

$$q \frac{\partial}{\partial t} (p - n) + \nabla \cdot (\bar{J}_n + \bar{J}_p) = 0, \quad (29)$$

where

$$q \frac{\partial}{\partial t} (p - n) = \frac{\partial \rho}{\partial t}.$$

Substituting the above expression for  $\frac{\partial}{\partial t} (p - n)$  into Eq. (29) and using Poisson's equation, we can obtain

$$\epsilon \frac{\partial}{\partial t} \nabla \cdot \bar{E} + \nabla \cdot (\bar{J}_n + \bar{J}_p) = 0. \quad (30)$$

Integration of Eq. (30) over the space coordinates leads to

$$\bar{J}(t) = \bar{J}_n + \bar{J}_p + \epsilon \frac{\partial \bar{E}}{\partial t}, \quad (31)$$

where  $\bar{J}(t)$  is the total current density, including the displacement current component  $\epsilon \frac{\partial \bar{E}}{\partial t}$ , and

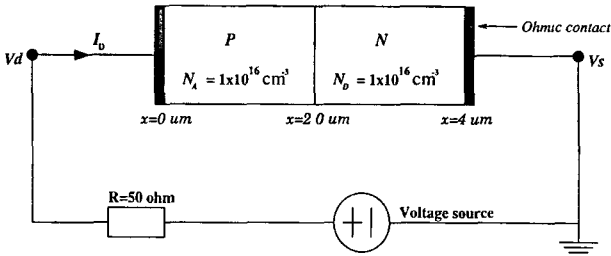


Fig. 5. A diode switching circuit for 2D mixed-level simulation.

$$\bar{I} = \int \bar{J} d\bar{S}, \quad (32)$$

where  $\bar{I}$  is the current in the circuit, and  $\bar{S}$  is the sample cross section (Shur, 1990).

## IV. Examples and Discussion

This section is devoted to discussing implementation and simulation in HSPICE using the model proposed in Section II. In order to verify the proposed model, a simple diode switching circuit shown in Fig. 5 is first used as an example of mixed-level simulation, including the charge storage effect. Another example is an SOS (Semiconductor-oxide-Semiconductor) structure simulation which will be helpful in modeling the semiconductor and insulator combination.

In the first example, the dopant impurity profile of the PN diode is  $N_A=1 \times 10^{16} \text{ cm}^{-3}$  in the p region and  $N_D=1 \times 10^{16} \text{ cm}^{-3}$  in the n region. Other parameters used in the program are as follows:  $n_i=1.5 \times 10^{10} \text{ cm}^{-3}$ , electron mobility  $\mu_n=1350 \text{ cm}^2/\text{V}\cdot\text{s}$ , hole mobility  $\mu_p=480 \text{ cm}^2/\text{V}\cdot\text{s}$ ,  $\tau_p=3 \times 10^{-6} \text{ s}$ , and  $\tau_n=1 \times 10^{-6} \text{ s}$ . The diode length is  $4 \mu\text{m}$ , and the cross area is  $1 \times 10^{-4} \text{ cm}^2$ . The source and drain contacts are both assumed to be ohmic. Grid modulation is used in the space-charge region, where a major change in electrostatic potential is expected. The simulation results are shown in Figs. 6 and 7. Figure 6 shows the input voltage function and the diode voltage waveform. It can be seen that the delay time caused by the minority-carrier storage-effect is about 9 ns. Figure 7 is the diode's current waveform during transient simulation of the diode switching circuit. It illustrates the diode recovery phenomenon due to the charge storage effect.

The next example investigates the mixed-level simulation of SOS structure (Fig. 8), which is essential for simulation of MOSFET, especially modeling of the gate-oxide region. The SOS sample has a length of  $6 \mu\text{m}$ , and the doping concentrations of the right side and

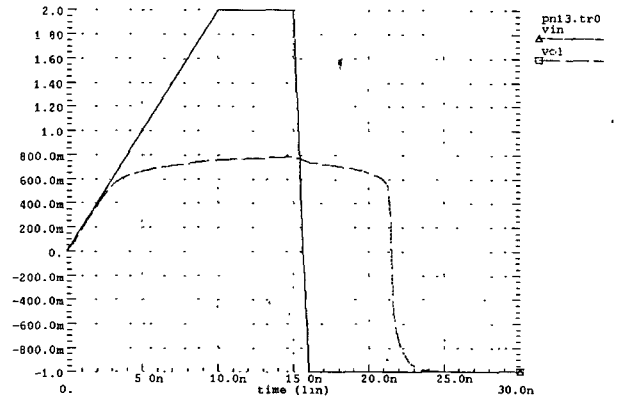


Fig. 6. The driving voltage waveform  $V_{in}$  and the voltage waveform across the diode  $V_{ol}$ . The vertical axis is for  $V_{in}$  and  $V_{ol}$  in mV. The horizontal axis is for time in ns.

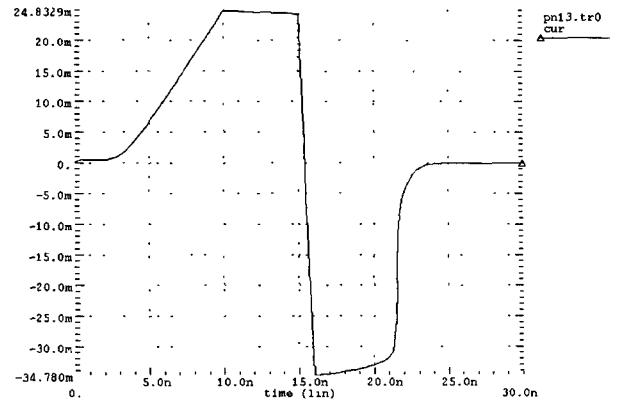


Fig. 7. The waveform of the diode current  $I_d$ . The vertical axis is for  $I_d$  in mA. The horizontal axis is for time in ns.

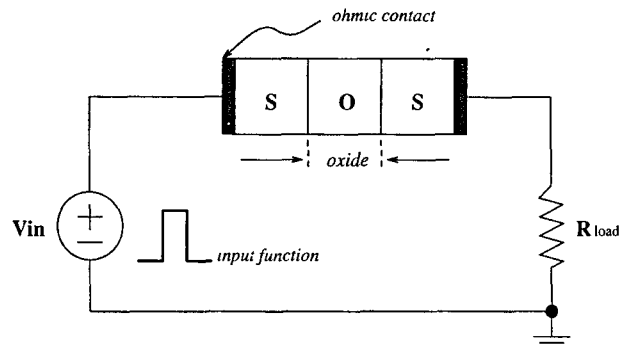


Fig. 8. The circuit diagram of R-C(SOS) transient mixed-level simulation.

left side semiconductors are all  $N_D=1 \times 10^{15} \text{ cm}^{-3}$ . Likewise, fine grids are used near the oxide-semiconductor interface to handle charge accumulation or depletion. The cross section area of the structure is

$1 \times 10^{-4} \text{ cm}^2$ , and the thickness of the oxide is  $6000 \text{ \AA}$ . The permittivity of the oxide is  $3.9 \times 8.85 \times 10^{-14} \text{ F/cm}$ , so the equivalent capacitor can be calculated by

$$C_{ox} = \frac{\epsilon A}{d}.$$

The value of the load resistor is  $1.5 \text{ k}\Omega$ , hence resulting in an  $RC$  time constant of nano-second scale. The displacement current component can be calculated as

$$J_d = \epsilon \frac{\partial F}{\partial t},$$

where  $F$  is the electric field ( $-\frac{\partial \psi}{\partial X}$ ), and  $\psi$  is the electrostatic potential. Figure 9 shows the input voltage function and voltage waveform of the SOS device, which includes the  $RC$  time delay character-

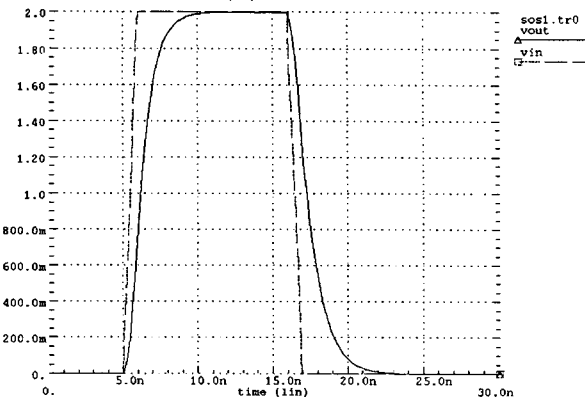


Fig. 9. The driving voltage waveform  $V_{in}$  and the voltage waveform across the SOS capacitor  $V_{out}$ . The vertical axis is for  $V_{in}$  and  $V_{out}$  in mV. The horizontal axis is for time in ns.

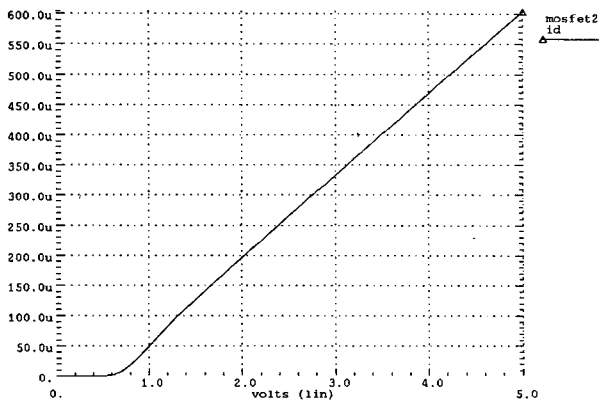


Fig. 10. The threshold voltage of MOSFET measured in the linear region using HSPICE. The vertical axis is for  $I_d$  in  $\mu\text{A}$ . The horizontal axis is for  $V_{gs}$  in V.

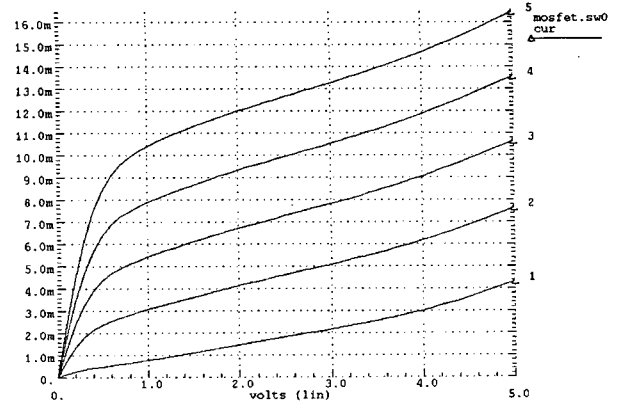


Fig. 11. The  $i$ - $v$  characteristic of MOSFET with  $0.8 \mu\text{m}$  channel length using HSPICE simulation. The vertical axis is for  $I_d$  in mA. The horizontal axis is for  $V_{ds}$  in V. The value of  $V_{gs}$  is shown at the right end of each  $i$ - $v$  curve.

istics.

The SOS modeling techniques can be applied to the MOS device. Consider an MOS structure with a  $p$ -type substrate doped to  $N_A = 1 \times 10^{16} \text{ cm}^{-3}$ , a gate doped to  $N_D = 2 \times 10^{16} \text{ cm}^{-3}$ , and a silicon-dioxide with a thickness of  $t_{ox} = 500 \text{ \AA}$ . The drain and source doping are both  $N_D = 1 \times 10^{18} \text{ cm}^{-3}$ , and the channel length is  $0.8 \mu\text{m}$ . Figure 10 illustrates the threshold voltage ( $V_{TO}$ ) characteristic in the linear region with  $V_{bs} = 0 \text{ V}$  and very small  $V_{ds}$ , in which  $V_{TO}$  approximates  $0.7 \text{ V}$ . Figure 11 shows the  $i$ - $v$  characteristics, where  $V_{gs}$  increases from  $1 \text{ V}$  to  $5 \text{ V}$  and  $V_{ds}$  sweeps from  $0 \text{ V}$  to  $5 \text{ V}$ . The short-channel effect is obvious when the drain voltage has a large bias. These examples prove that the methodology we have proposed is feasible for 2D mixed-level simulation.

## V. Conclusion

In this paper, an equivalent circuit approach to two-dimensional mixed-level device and circuit simulation using HSPICE has been presented. A PN diode switching circuit and SOS test circuit have been used as examples to verify this algorithm. The modeling technique has also been successfully applied to sub-micron MOSFET device simulation. Thus, this approach has been proved to be useful for mixed-level circuit/device simulation and applicable to any device if the user can properly model the device physics in the equivalent circuit. It is helpful for detailed simulation of some small electronic circuits, critical devices, or portions of larger circuits.

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# 用HSPICE研究二維元件與電路之混階模擬

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## 摘 要

本篇文章研究以等效電路模型法在HSPICE上作二維元件和電路的混階模擬。所謂等效電路模型法，就是將傳統用來描述元件載子傳輸的模型轉換成等效電路模型。如此一來，元件模擬變成了電路模擬，不但可用電路模擬器來做元件模擬而且可以和一般的電路結合，形成混階模擬。首先，我們先推導二維的等效電路模型，然後裝入HSPICE中，並以二極體切換電路為例子作混階模擬，探討因少數載子儲存效應所造成的延遲時間。接下來是SOS（semiconductor-oxide-semiconductor）元件的模擬，並將此技術應用於次微米金氧半結構之元件上。此方法有助於我們更深入了解元件或製程參數對電路特性的影響，以及元件在實際電路所造成的動態邊界條件下的特性變化。